REMARKS

Claims 9-18 are pending. Claims 1-8 and 19-23 have been canceled only as being drawn to non-elected claims and without prejudice. Applicant reserves the right to reintroduce such claims later in prosecution or in a continuation application. Claim 9 has been amended for clarity. Reconsideration of the application in light of the above amendments and the following remarks is respectfully requested.

I. REJECTION OF CLAIMS 9-18 UNDER 35 U.S.C. § 103(a)

Claims 9-18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Ouyange et al. (US publication 2004/0256639) in combination with Lin et al. (US publication 2005/0035369), Yeo et al. (US publication 2005/009263), Chidambarrao et al. (US publication 2005/0164477), and Currie et al. (US publication 2004/0173812). Withdrawal of the rejection is respectfully requested for at least the following reason.

A prima facie case of obviousness requires that the cited references teach or suggest all of the claim limitations and also that some suggestion or motivation to combine the references be available.

Claim 9 recites forming PMOS devices with entire source to drain channel regions formed *within the substrate along a first crystallographic orientation* and NMOS devices with entire source to drain channel regions formed *within the substrate along a second crystallographic orientation*, which is not taught by the cited references.

The Office Action relies upon Ouyang et al. to teach the elements of claim 9. Ouyang et al. disclose a method for forming a *vertical channel* of a field effect transistor. (Abstract). The source region and channel region are independently lattice strained with respect to the body region (substrate). (Abstract). Only the drain region 162 is formed within the substrate below other portions of the vertical column or mesa 5000. (Fig. 5, 6, and 7). The vertical column 5000 comprises the source region 164, a body region 163, a drain region 162 and has a channel region 165 on sidewalls of the

vertical column 5000. [0030] In contrast, the entire source to drain channel regions, source regions, and drain regions of claim 9 are formed within the substrate.

Ouyang et al. do suggest a mesa or vertical structure orientation where a portion of the p-channel is in the plane (110) and a portion of the n-channel is in the plane (100). [0083] However, the *entire* n-channel is not along the plane (100) as recited in claim 9. (Fig. 5). More particularly, Ouyang et al. teach rotating a vertical structure of an nMOSFET device by 45 degrees. [0049] As a result, the n-channels on all the sidewalls of the vertical structure are along four different planes (001), (010), (001), and (010) as shown in Fig. 8B as opposed to a single, entire channel along a single crystallographic orientation as in claim 9. [0049] Similarly, the pMOSFET device of Ouyang et al. has p-channels on sidewalls of the vertical structure along planes (011), (011), (011), and (011).

Therefore, it can be seen that Ouyang fail to teach forming PMOS devices with entire source to drain channel regions formed within the substrate along a first crystallographic orientation and NMOS devices with entire source to drain channel regions formed within the substrate along a second crystallographic orientation as recited in claim 9. The other references fail to cure this deficiency of Ouyang et al.

Additionally, it is noted that the vertical channels and source regions are not formed within the substrate as in claim 9. The vertical channels 165 are at least partially formed along sidewalls of the vertical structures 5000 and the source region is a composite of a poly silicon layer 410 formed on top of a strained SiGe layer 164 in the vertical channel 5000 and over the substrate 161. [0030, 0040]

As a result, Ouyang et al. and the other cited references, alone or in combination, fail to teach or suggest all the elements of claim 1. Claims 10-18 depend from claim 9 and are not taught by the cited references for at least the above reasons. Accordingly, withdrawal of the rejection is respectfully requested.

II. CONCLUSION

For at least the above reasons, the claims currently under consideration are believed to be in condition for allowance.

Should the Examiner feel that a telephone interview would be helpful to facilitate favorable prosecution of the above-identified application, the Examiner is invited to contact the undersigned at the telephone number provided below.

Authorization is hereby given to the Commissioner to charge a one-month extension of time fee, as well as any other fees due as a result of the filing of this response to Deposit Account Number 20-0668, TI-36595.

Respectfully submitted,
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CERTIFICATE OF MAILING (37 CFR 1.8a)

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop AF, Assistant Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date: December 14, 2005

Christine Gillroy
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